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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,479	08/03/2001	Thomas Zettler	J&R-0694	7212
24131 7590 11/01/2007 LERNER GREENBERG STEMER LLP			EXAMINER	
P O BOX 2480		CHUNG, PHUNG M		
HOLLYWOOD, FL 33022-2480			ART UNIT	PAPER NUMBER
			2117	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)			
	09/922,479	ZETTLER, THOMAS			
Office Action Summary	Examiner	Art Unit			
	Phung My Chung	2117			
The MAILING DATE of this communication appears on the cover sheet with the correspondence address Period for Reply					
A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication. - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).					
Status					
Responsive to communication(s) filed on <u>20 Au</u> This action is FINAL . 2b)⊠ This Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, pro				
Disposition of Claims					
4)	rn from consideration.				
Application Papers					
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) access Applicant may not request that any objection to the Replacement drawing sheet(s) including the correction of the oath or declaration is objected to by the Examine 10.	epted or b) objected to by the Eddrawing(s) be held in abeyance. See ion is required if the drawing(s) is obj	e 37 CFR 1.85(a). jected to. See 37 CFR 1.121(d).			
Priority under 35 U.S.C. § 119					
 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f). a) All b) Some * c) None of: 1. Certified copies of the priority documents have been received. 2. Certified copies of the priority documents have been received in Application No. 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)). * See the attached detailed Office action for a list of the certified copies not received. 					
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date	4) Interview Summary Paper No(s)/Mail Da 5) Notice of Informal P 6) Other:	ate			

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DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because all rectangular boxes in Figs. 1 and 12 should be labeled with numbers and elements to clearly indicate which numbers or elements the boxes represent. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the external testing device and all of the method steps, for example,

Providing an integrated circuit...;

Starting to perform a test...;

Taking at least parts of the integrated circuit out of operation...;

Subsequently, connecting the integrated circuit to an external testing device...;...

must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. *Any amended*replacement drawing sheet should include all of the figures appearing on the

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immediate prior version of the sheet, even if only one figure is being amended.

The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

INFORMATION ON HOW TO EFFECT DRAWING CHANGES

Replacement Drawing Sheets

Drawing changes must be made by presenting replacement sheets which incorporate the desired changes and which comply with 37 CFR 1.84. An explanation of the changes made must be presented either in the drawing amendments section, or remarks, section of the amendment paper. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). A replacement sheet must include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of the amended drawing(s) must not be labeled as "amended." If the changes to the drawing figure(s) are not accepted by the examiner, applicant will be notified of any required corrective action in the next Office action. No further drawing submission will be required, unless applicant is notified.

Identifying indicia, if provided, should include the title of the invention, inventor's name, and application number, or docket number (if any) if an application number has not

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been assigned to the application. If this information is provided, it must be placed on the front of each sheet and within the top margin.

Annotated Drawing Sheets

A marked-up copy of any amended drawing figure, including annotations indicating the changes made, may be submitted or required by the examiner. The annotated drawing sheet(s) must be clearly labeled as "Annotated Sheet" and must be presented in the amendment or remarks section that explains the change(s) to the drawings.

Timing of Corrections

Applicant is required to submit acceptable corrected drawings within the time period set in the Office action. See 37 CFR 1.85(a). Failure to take corrective action within the set period will result in ABANDONMENT of the application.

If corrected drawings are required in a Notice of Allowability (PTOL-37), the new drawings MUST be filed within the THREE MONTH shortened statutory period set for reply in the "Notice of Allowability." Extensions of time may NOT be obtained under the provisions of 37 CFR 1.136 for filing the corrected drawings after the mailing of a Notice of Allowability.

Claim Rejections - 35 USC § 103

- 2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 3. Claims 1-4, 6 and 9-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phan (6,651,202) in view of Karimi et al (6,574,762).

As per claims 1-2 and 9, Phan discloses the invention substantially as claimed, comprising the steps of:

Providing an integrated circuit (integrated circuit IC) that includes a self-test device (BIST/BISR);

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Starting to perform a test of the integrated circuit with the self-test device (diagnosis of the integrated circuit IC by the BIST/BISR circuitry is performed upon an initial power up) (col.9, lines 51-59);

Taking at least parts of the integrated circuit out of operation after the parts have been tested by the self-test device (col. 10, lines 61-67 to col. 11, lines 1-11); and Connecting the integrated circuit to an external testing device that performs a function selected from the group consisting of reading out results of the test and evaluating the results of the test. (See col. 9, lines 44-64 and col. 3, lines 43-45). Phan does not specifically disclose that the built-in self test circuit for self testing before connecting to the external test device. However, Phan's BIST starting to perform a test of the integrated circuit with the self-test device upon an initial power up (col.9, lines 51-59) **or** when initiated by the external device (col. 9, lines 53-59). Therefore, it is assume that the BIST of Phan can be operate for self testing before connecting or transferring test results to the external device. However, it would have been a mater of design choice to a person of ordinary skill in the art, at the time the invention was made to complete the self test before connecting and transferring the test results to the external test device upon power is ON or to connect the external test device before the self test operation to receive control clock signal from the external test device before initiate the self test as desired when needed.

As per claim 3, Phan further discloses which comprises at least partially completing the test while performing a function selected from the group consisting of

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temporarily storing the integrated circuit and transporting the integrated circuit to the external testing device. (See col. 9, lines 44-64).

As per claim 4, Phan further discloses providing a self test control device that causes performance of the test of the integrated circuit; and

Moving the control device together with the integrated circuit. (See col. 6, lines 20-45).

As per claim 6, Phan further discloses with the self test device, writing data into a test result memory; and after testing the integrated circuit (IC), taking out of operation, components of the IC that are not needed to continue to store the data in the test result memory is inherent in the multiplexing circuitry of Phan. (See (See col. 9, lines 44-64, col. 3, lines 43-45 and col. 10, lines 61-67 to col. 11, lines 1-11):

As per claim 10, Phan further discloses providing the integrated circuit on at least one wafer. (Col. 10, lines 35-39).

As per claims 11-15, these claims are rejected under similar rationale as set forth in claims 1-3.

4. Claims 7-8, 16-17, 19-23 and 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Phan (6,651,202) in view of Karimi et al (6,574,762).

As per claim 7, the teaching of Phan has been discussed above. Phan does not specifically disclose preventing a clock signal from being supplied to the parts of the integrated circuit. However, Karimi et al disclose preventing a clock signal from being supplied to the parts of the integrated circuit (Fig. 1, col. 7, lines 57-65 and col. 8, lines 4-12). Therefore, it would have been obvious to a person of ordinary skill in the art, at

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the time the invention was made, to incorporate the step of preventing a clock signal from being supplied to the parts of the integrated circuit as taught by Karimi et al into the invention of Phan to prevent the clock signal from being applied to the part of integrated circuit that has been taken out of operation.

As per claim 8, this claim is rejected under similar rationale as set forth in claim 7.

As per claims 16-17, 19-23 and 29-30, these claims are rejected under similar rational as set forth in claims 1-4, 6-8 and 9-15.

- 5. Applicant's arguments dated on 8/20/07 with respect to claims 1-4, 6-23 and 29 have been considered but are most in view of the new ground(s) of rejection.
- 6. Applicant's arguments filed on 11/02/05 have been fully considered but they are not persuasive because applicant argues that Phan teaches that the built-in self test circuit must connected to the external test device (ATE 160) to operate (Phan specifically teahes that the external clock controlling BIST operation is supplied by the external test device see col. 8, lines 5-18).

Examiner disagrees with applicant because Phan's BIST starting to perform a test of the integrated circuit with the self-test device upon an initial power up (col.9, lines 51-59) <u>or</u> when initiated by the external device (col. 9, lines 53-59). Therefore, it is assume that the BIST of Phan can be operate for self testing before connecting or transferring test results to the external device. However, it would have been a mater of design choice to a person of ordinary skill in the art, at the time the invention was made to complete the self test before connecting and transferring the test results to the

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external test device upon power is ON to reduce test time or to connect the external test device before the self test operation to receive control clock signal from the external test device before initiate the self test as desired when needed.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phung My Chung

Primary Patent Examiner

Art (1/2)